IN THE SPECIFICATION:

Please amend the specification as follows:

Please substitute the paragraph beginning at page 16, line 19, with the following.

-- In step S002, the positions of marks WAP (see, for example, Figs. 1 and 6) formed in two shots on the wafer WF held by the wafer chuck WS are detected by the off-axis scope OE. On the basis of the detection results, the stages XYS and θS are driven to coarsely set the wafer WF at the reference position. --

Please substitute the paragraph beginning at page 25, line 2, with the following.

-- Fig. 7 is a view schematically showing the relationship between the off-axis scope (OE), reduction projecting lens (LN), target stage driving position, and actual stage driving position (average position). The base line bloas represents the offset value between the optical axis of the reduction projecting lens and that of the off-axis scope. In step movement for actual exposure, the stage is driven in consideration of this offset value. The average deviations dx and dy are small values in fact, though they have large values in Fig. 7 for ~~the~~ descriptive convenience. --

Please substitute the paragraph beginning at page 29, line 5, with the following.

-- In the second step (S104 and S105), the exposure shutter is opened, and a pattern drawn on a reticle RT held by a reticle stage RS is projected onto the resist applied to the wafer WF through a projecting lens LN to expose it (S104). More specifically, light from a light source

IL is incident on the projecting lens LN through a masking blade ~~MB~~ SHT and reticle Rt. The image of the pattern formed on the reticle RT is reduced to 1/5 by the projecting lens LN and projected onto the resist applied to the wafer WF. At this time, the pattern of an alignment mark to be used in the fourth step is formed on the resist by exposure. This exposure is executed for all shots while moving an XY stage XYS. --

Please substitute the paragraph beginning at page 30, line 10, with the following.

-- The positions of alignment marks WML and WMR in each shot are measured by the TTL off-axis scheme, and global alignment is performed on the basis of the measurement results (S109). More specifically, non-exposure light emitted by non-exposure light source LSY (see, for example, Fig. 8), e.g., a HeNe laser is transmitted through a half mirror HM, reflected by a mirror MRA, and transmitted through the projecting lens LN to irradiate the alignment mark WML on the wafer WF. The non-exposure light reflected by the wafer WF is transmitted through the projecting lens LN, reflected by the mirror MRA, and transmitted through the half mirror HM to be incident on a CCD camera CMY (see, for example, Fig. 2). With this operation, the image of the alignment mark WML is formed on the imaging plane of the CCD camera CMY. Next, the XY stage XYS is moved to form the image of the alignment mark WMR formed on the opposite side of the alignment mark WML on the imaging plane of the CCD camera CMY. --

Please substitute the paragraph beginning at page 37, line 5, with the following.

-- First, in step SAS011, a stage deviation storage section 400 determines on the basis of target position data of the stage 900 whether the stage 900 has reached a position (observation area) where the image sensing section (OE) 700 can observe a corresponding mark. If YES in step ~~SAS001~~ SAS011, the stage deviation storage section 400 sends a sync signal for starting observation to the image sensing control section 300 in step SAS012. --

Please substitute the paragraph beginning at page 38, line 10, with the following.

-- On the other hand, the image sensing control section 300, which ~~is monitoring reception of a syn signal~~ monitors reception of a sync signal in step SAC011, receives the sync signal from the stage deviation storage section 400 and recognizes that the stage deviation storage section 400 has started storing the position of the stage 900, and the flow advances to step SAC012. --

Please substitute the paragraph beginning at page 41, line 4, with the following.

-- In step S1 (circuit design), the circuit of a semiconductor device is designed. In step S2 (mask preparation), a mask having the designed circuit pattern is prepared. --

Please substitute the paragraph beginning at page 41, line 8, with the following.

-- In step S3 (wafer manufacturing), a wafer is manufactured using a material such as silicon. In step S4 (wafer process), called a preprocess, an actual circuit is formed on the wafer by lithography using the prepared mask and wafer. --

Please substitute the paragraph beginning at page 41, line 13, with the following.

-- In step S5 (assembly), called a post-process, a semiconductor chip is formed from the wafer prepared in step S4. This step includes processes such as assembly (dicing and bonding) and packaging (chip encapsulation). --

Please substitute the paragraph beginning at page 41, line 17, with the following.

-- In step S6 (inspection), inspections including an operation check test and a durability test of the semiconductor device manufactured in step S5 are performed. A semiconductor device is completed with these processes and delivered (step S7). --

Please substitute the paragraph beginning at page 41, line 22, with the following.

-- Fig. 13 shows a detailed flow of the wafer process. In step S11 (oxidation), the surface of the wafer is oxidized. In step S12 (CVD), an insulating film is formed on the wafer surface. --

Please substitute the paragraph beginning at page 41, line 26, and ending on page 42, line 6, with the following.

-- In step S13 (electrode formation), an electrode is formed on the wafer by deposition. In step S14 (ion implantation), ions are implanted into the wafer. In step S15 (resist process), a photosensitive material is applied to the wafer. In step S16 (exposure), the circuit pattern of the mask is printed on the wafer by exposure using the above-described exposure apparatus. --

Please substitute the paragraph beginning at page 42, line 7, with the following.

-- In step S17 (development), the exposed wafer is developed. In step S18 (etching), portions other than the developed resist image are etched. In step S19 (resist peeling), unnecessary resist remaining after etching is removed. By repeating these steps, a multilayered structure of circuit patterns is formed on the wafer. --